EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	3975	(floating adj gate) and (control adj gate) and source and drain and ((implanting or implantation or doping or doped) same mask)	US-PGPUB; USPAT	OR	ON	2006/05/31 17:08
L3	897	2 and @ad<"19970411"	US-PGPUB; USPAT	OR	ON	2006/05/31 17:19

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	6598	(floating adj gate) and (control adj gate) and drain and source and (doping or implantation or implanting)	US-PGPUB; USPAT	OR	ON	2006/05/31 13:01
L2	2154	1 and @ad<"19981110"	US-PGPUB; USPAT	OR	ON	2006/05/31 12:48
L3	1727	2 and electrons	US-PGPUB; USPAT	OR	ON	2006/05/31 13:01
L4	1695	3 and memory	US-PGPUB; USPAT	OR	ON	2006/05/31 12:50
L5	1513	3 and (memory adj cells)	US-PGPUB; USPAT	OR	ON	2006/05/31 12:50
L6	576	(floating adj gate) and (control adj gate) and drain and source and (doping or implantation or implanting)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/31 13:01
L7	67	6 and electrons	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/31 13:01

US-PAT-NO: 6114724

DOCUMENT-IDENTIFIER: US 6114724 A

TITLE: Nonvolatile semiconductor memory cell with select gate

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Brief Summary Text - BSTX (5):

A cross-section of a typical conventional EEPROM cell 100 is shown in FIG. 1A. EEPROM cell 100 is formed on semiconductor substrate 102 and includes a select transistor 124 and a floating gate transistor 122. Select transistor 124 includes source region 106, drain region 108, gate oxide 112 and select gate 116. Floating gate transistor 122 includes source region 104, drain region 106 (which it shares with select gate 106), tunnel oxide 110, floating gate 118, interlayer dielectric 114, and control gate 120. Erasing of floating gate transistor 122 is typically accomplished by storing negative charge on floating gate 118. This may be accomplished by applying a large positive voltage to control gate 120 and grounding regions 104 and 106 such that **electrons** may tunnel through tunnel oxide 110 to floating gate 118. Programming of floating gate transistor 122 may be accomplished by applying a large positive voltage to select gate 116 (e.g., 15-20 volts), applying a large positive voltage to drain region 108, applying ground to control gate 120, and floating source region 104. In this configuration, **electrons** may tunnel from floating gate 118 to region 106 through tunnel dielectric 118 to create a positive charge on floating gate 118.

Brief Summary Text - BSTX (7):

formation of two different oxide thicknesses. Tunnel oxide 110 generally needs to be thin enough to enable **electron** tunneling (e.g., less than 125 angstroms). Gate oxide 112 is generally significantly thicker (e.g., 200 to 500 angstroms) than tunnel oxide 110 as gate oxide 112 must be able to withstand the high positive program voltages supplied to select gate 116 without breaking down. Forming two different oxide thicknesses generally increases the complexity and cost of forming EEPROM cell 100. U.S. Pat. No. 5,471,422 discloses an EEPROM cell that uses only tunnel oxide 110 in the formation of its floating gate and select gate transistors.

Detailed Description Text - DETX (9):

FIGS. 5-11 show one method of forming EEPROM cell 300 according to the

present invention. Other methods may be used to form EEPROM cell 300. As shown in FIG. 5, a tunnel dielectric layer may be formed over semiconductor substrate 302. Tunnel dielectric layer 502 may be grown or deposited by any process generally known for such formation. For example, tunnel dielectric layer 502 may be thermally grown from a silicon substrate 302. Tunnel dielectric layer 502 may be formed from any dielectric material(s) suitable for use as a tunnel dielectric (e.g., silicon dioxide). Tunnel dielectric layer 502 may be any thickness that enables **electron** tunneling with appropriate voltage ranges described below. Preferably, tunnel dielectric layer 502 is less than 150 .ANG., and more preferably less than 100 .ANG..

Detailed Description Text - DETX (19):

Erasing a state stored on floating gate 314 may be accomplished by applying appropriate voltages to the terminals of floating gate transistor 326 such that floating gate 314 is at a much more positive potential compared to the inversion layer linking regions 306 and 304 formed due to the positive potential on layer 314. For example, select gate transistor 328 passes a zero or negative potential on 308 by applying a suitable bias on gate 316. Floating gate 314 may then be erased using Fowler-Nordheim tunneling by applying approximately 0 volts to region 304 (or allowing it to float), and approximately 15 to 18 volts to control gate 322. A high electric field may then be created across tunnel dielectric layer 310 such that **electrons** may flow from the channel region, region 306, and region 304, to floating gate 314. To reduce the positive voltage on control gate 322, a negative voltage may be applied to regions 308 and 302 as shown in Erase Scheme B in Table 1. Erase Scheme B may be used, for example, in a cell formed by the triple-well process shown in FIG. 3B. One or more EEPROM cells may be erased at the same time. It may take approximately 1 to 10 milliseconds (ms) to perform an erase function. This time may be amortized over the number or EEPROM cells that may be erased at one time.

Detailed Description Text - DETX (20):

Programming data or charge onto floating gate 314 may be accomplished by enabling select gate transistor 328 and applying appropriate voltages to the terminals of floating gate transistor 326. Select gate transistor 328 may be enabled by applying and approximately 4 to 7.0 volts on gates 324 and 316. Approximately 3 to 5.5 volts may then be applied to region 308 (bit line 1202) such that approximately 3 to 5.5 volts may be present at region 306. This range of voltages is significantly reduced relative to the higher voltages generally used by conventional EEPROM cells. Floating gate 314 may then be programmed using Fowler-Nordheim tunneling by floating region 304 and applying approximately -7 to -12 volts to control gate 314. A high electric field may

then be created across tunnel dielectric layer 310 such that **electrons** may flow from floating gate 314 to drain region 306. One or more EEPROM cells (e.g., in the same row) may be programmed at the same time. It may take approximately 1 to 10 milliseconds (ms) to perform a program function. This time may be amortized over the number or EEPROM cells that may be programmed at one time.

Detailed Description Text - DETX (21):

EEPROM cell may be programmed using a small amount of current and a small amount of power. For one embodiment, EEPROM cell 300 may require from approximately 10 nanoamperes (nA) of current to program EEPROM cell 300. Most of this current may flow from region 306 to region 302 due to band-to-band tunneling caused by high vertical fields on the tunnel dielectric. If the operating power supply is approximately 3 to 5 volts, then it may require approximately 30 nanoWatts (nW) to 50 nW to program EEPROM cell 300. The low programming current may be a result of the **electron** injection efficiency (i.e., the ratio of gate current to drain current injected into drain region 306) of using Fowler-Nordheim tunneling as opposed to other programming techniques such as hot **electron** injection. For one embodiment, the **electron** injection efficiency may be approximately 10.sup.-3 to 10.sup.-4.